WHAT IS CLAIMED IS:

1. A data converter, implemented as an integrated circuit device, comprising:

signal processing circuitry operable to produce an output signal in dependence upon a received input signal, production of the output signal being initiated at a time determined by a timing signal and being completed at a time which is delayed by a delay time with respect to said timing signal, said signal processing circuitry comprising a delay-contributing portion which makes a contribution to said delay time that is affected by variations in a power supply voltage applied to the delay-contributing portion; and

an internal supply voltage regulator, connecting to, when the device is in use, a power source external of the device to receive therefrom an external power source voltage, and operable to derive from the external power source voltage a regulated internal power supply voltage which is applied to said corresponding delay-contributing portion so as to fix said contribution at some value independent of variations in said external power source voltage, at least one further circuitry portion within the device being powered by a supply voltage other than said regulated internal power supply voltage.

2. A data converter as claimed in claim 1, wherein said internal supply voltage regulator serves exclusively to power said delay-contributing portion alone.

3. A data converter as claimed in claim 1, wherein said delay-contributing portion is a clock input portion.

4. A data converter as claimed in claim 3, wherein said clock input portion is operable to receive said timing signal and to derive therefrom at least one internal clock signal for use by said signal

processing circuitry.

5. A data converter as claimed in claim 1, wherein said delay-contributing portion is a clock distribution portion.

6. A data converter as claimed in claim 5, wherein said clock distribution portion is operable to distribute one or more clock signals derived from said timing signal within said signal processing circuitry.

7. A data converter as claimed in claim 1, wherein said delay-contributing portion is a latch portion.

8. A data converter as claimed in claim 7, wherein said latch portion is operable to latch a signal at a time determined by a clock signal to produce a clocked signal which is used in the production of said output signal.

9. A data converter as claimed in claim 1, wherein said delay-contributing portion is a switch driver portion.

10. A data converter as claimed in claim 9, wherein said switch driver portion is operable to receive a control signal and to produce a driving signal for application to a switch to open and close said switch in response to changes in the received control signal.

11. A data converter as claimed in claim 9, wherein said switch is opened and closed to change a sample-and-hold circuit between a sampling state and a holding state.

12. A data converter as claimed in claim 1, wherein said delay-contributing portion is an electronic switch portion.

13. A data converter as claimed in claim 12, wherein said electronic switch portion is used to switch the whole or part of said output signal.

14. A data converter as claimed in claim 1,

wherein said delay-contributing portion is an analog amplifier portion.

15. A data converter as claimed in claim 1, wherein said signal processing circuitry operates repetitively to perform a series of processing cycles, and one such output signal is produced in each said processing cycle.

16. A data converter as claimed in claim 1, wherein at least one circuitry portion of said signal processing circuitry is divided into a plurality of circuitry segments which are operable in combination to produce said output signal in dependence upon said received input signal.

17. A data converter as claimed in claim 16, wherein each circuitry segment comprises one said delay-contributing portion and a corresponding internal supply voltage regulator deriving a regulated internal power supply voltage from an external power source and applying that regulated internal power supply voltage to the delay-contributing portion in its circuitry segment.

18. A data converter as claimed in claim 1, comprising two or more sets of said signal processing circuitry, wherein each said set of signal processing circuitry has its own said internal supply voltage regulator for applying a regulated internal power supply voltage to such a delay-contributing portion in the set of signal processing circuitry concerned.

19. A data converter as claimed in claim 1, wherein said signal processing circuitry comprises:

a decoder which receives said input signal in digital form and decodes the input signal to produce one or more decoded signals; and

analog circuitry responsive to said one or more decoded signals to produce said output signal in analog form.

20. A data converter as claimed in claim 19, wherein said signal processing circuitry further comprises one or more latches connected between the decoder and the analog circuitry and operative to latch said one or more decoded signals.

21. A method of controlling power-supply-dependent jitter in a data converter implemented as an integrated circuit device, the data converter comprising signal processing circuitry operable to produce an output signal in dependence upon a received input signal, and production of the output signal being initiated at a time determined by a timing signal and being completed at a time which is delayed by a delay time with respect to said timing signal, said method comprising:

employing a supply voltage regulator, internal to the device, to derive a regulated internal power supply voltage from an external power source voltage supplied to the device by a power source external of the device;

applying the regulated internal power supply voltage to a delay-contributing portion which forms part of said signal processing circuitry and which makes a contribution to said delay time that is affected by variations in a power supply voltage applied thereto, so as to fix said contribution at some value independent of variations in said external power source voltage; and

powering at least one further circuitry portion within the device by a supply voltage other than said regulated internal power supply voltage.